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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,554	01/30/2002	Douglas Hooker Bradley	AUS920010743US1	5802

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EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/059,554	BRADLEY ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations "a select circuit configured...the carry-out bit" in line 10-11 in claim 1 and limitations cited in claims 5-6 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the abstract exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 10 and 20 are objected to because of the following informalities:

Re claims 10 and 20, these two claims cite a limitation that is very same to the limitation (lines 10-11) of claims 1 and 20 respectively, despite some slight wording. The applicant is advised to either cancel the claims 10 and 20 to avoid duplication or amend these claims to distinguish from claims 1 and 20.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Hayakawa (U.S. Patent Application No.: 2001/0037349A1).

Re claim 1, Hayakawa discloses in Figure 19 an adder circuit for determining the sum of two operands (e.g. left column page 1 paragraph 0008), comprising: a set of PGK (Figure 19 to product K0-K31, P0-G31, and G0-G31 prior entering Stage-0) circuits configured to generate propagate (P), generate (G), and kill (K) bits corresponding to at least a portion of the first and second operands (e.g. a and b operands in left column page 1 paragraph 0008); at least one tier of group circuits (e.g. Stage-0 in Figure 19) configured to receive the propagate, generate, and kill bits from a plurality of the PGK circuits and to produce, in response thereto, a set of group propagate, generate, and kill values (output of all 4-bit CLA); a carry generation circuit (Stage-2) configured to receive a carry-in bit (e.g. Cin and bar(Cin) in Stage-2) and the outputs of at least one of the group circuits (e.g. PGGG/GGG/KGGG) and further configured to generate a carry-out bit (C<31> in Stage-2) representing the carry-out of the corresponding group; and a select circuit (e.g. left column page 1 paragraph 0008) configured to select between a first sum and a second sum responsive to the carry-out bit.

Re claim 2, Hayakawa further discloses in Figures 21 each generate bit is the logical AND of its corresponding bits in the first and second operand (Figure 21(c)), each

propagate bit is the EXOR of its corresponding bits in the first and second operands (Figure 21(a)), and each kill bits is the logical NOR of its corresponding bits in the first and second operands (Figure 21(b)).

Re claim 3, Hayakawa further discloses in Figure 21 at least one of the PGK circuits, group circuits, and carry circuits includes at least one CMOS transmission gate (e.g. any Figure in Figures 21).

Re claim 4, Hayakawa further discloses in Figure 19 the PGK circuits, group circuits, and carry circuits are implemented primarily with CMOS transmission gates (e.g. 0024 in page 2).

Re claim 5, Hayakawa further discloses in Figures 19 and 21 the PGK circuits farther generate the logical complements of the propagate, generate, and kill bits substantially simultaneously with the generation of the propagate, generate, and kill bits (Figures 19 and 21(a)-21(c).

Re claim 6, Hayakawa further discloses in Figure 19 the group circuits further generate the logical complements of the group propagate, generate, and kill values (e.g. 0147 in page 9).

Re claim 7, Hayakawa further discloses in Figure 19 the PGK and group circuits are implemented primarily with CMOS transmission gates (e.g. all the Figures are disclosed with CMOS).

Re claim 8, Hayakawa further discloses in Figure 19 the at least one tier of group circuits (e.g. Stage-0; Stage-1; Stage-2) includes a first tier of group circuits configured to receive the output of the PGK circuits and to generate an intermediate set of group

propagate, generate, and kill values (e.g. Stage-1) and a second tier (e.g. Stage-2) of at least one group circuit configured to receive the intermediate set of group propagate, generate, and kill values and to produce a final group propagate, generate, and kill values.

Re claim 9, Hayakawa further discloses in Figure 19 the intermediate group of propagate, generate, and kill values (e.g. PGG, GGG< KGG) each corresponds to a group of four adjacent bits and further wherein the final group of propagate, generate, and kill values correspond to a group of 16 adjacent bits (e.g. first 4-bit CLA corresponding to first 16 bits).

Re claim 10, Hayakawa further discloses in Figure 19 the carry-out bits generated by each of the carry generation circuits (e.g. C<31>) is used to select between a first sum and a second sum (e.g. 0008 in page 1).

Re claim 11, it is a microprocessor claim of claim 1. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 12, it is a microprocessor claim of claim 2. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 13, it is a microprocessor claim of claim 3. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 14, it is a microprocessor claim of claim 4. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 15, it is a microprocessor claim of claim 5. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 16, it is a microprocessor claim of claim 6. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 17, it is a microprocessor claim of claim 7. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 18, it is a microprocessor claim of claim 8. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 19, it is a microprocessor claim of claim 9. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 20, it is a microprocessor claim of claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,742,014 to Bradley discloses a conditional carry encoding for carry select adder.

b. U.S. Patent No. 5,270,955 to Bosshart et al. disclose a method of detecting arithmetic or logical computation result.

c. U.S. Patent No. 5,719,803 to Naffziger discloses a high speed addition using Ling's equations and dynamic CMOS logic.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

November 15, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100